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Silicon@-on-porous silicon@ prodn. - by anodisation followed by ion implantation to produce amorphous structure, suitable for making SOI devices

Patent Assignee: UK SEC FOR DEFENCE (MINA)
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Number of Countries: 017 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9209104	A1	19920529	WO 91GB2029	A	19911118	199224	B
EP 558554	A1	19930908	EP 91920076	A	19911118	199336	
			WO 91GB2029	A	19911118		
GB 2271465	A	19940413	WO 91GB2029	A	19911118	199413	
			GB 937147	A	19930406		
JP 6502280	W	19940310	JP 91518117	A	19911118	199415	
			WO 91GB2029	A	19911118		
GB 2271465	B	19941026	WO 91GB2029	A	19911118	199440	
			GB 937147	A	19930406		
US 5387541	A	19950207	WO 91GB2029	A	19911118	199512	
			US 9350401	A	19930511		

Priority Applications (No Type Date): GB 9025236 A 19901120
Cited Patents: 3.Jnl.Ref; EP 312466; JP 59144149
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9209104	A1	E	24	H01L-021/76	
Designated States (National): CA GB JP US					
Designated States (Regional): AT BE CH DE DK ES FR GB GR IT LU NL SE					
EP 558554	A1	E		H01L-021/76	Based on patent WO 9209104
Designated States (Regional): AT BE CH DE DK ES FR GB GR IT LI LU NL SE					
GB 2271465	A			H01L-021/265	Based on patent WO 9209104
JP 6502280	W		12	H01L-021/20	Based on patent WO 9209104
GB 2271465	B			H01L-021/265	Based on patent WO 9209104
US 5387541	A		10	H01L-021/302	Based on patent WO 9209104

Abstract (Basic): WO 9209104 A

Prodn. comprises: (a) mfg. a porous Si layer on a suitable Si wafer such that the Si wafer has a porous Si surface and a non-porous Si surface; and (b) applying an implanted ion dose to at least a portion of the porous Si surface such that the dose is sufficient to cause amorphisation of porous Si.

USE/ADVANTAGE - Used for producing electronic devices of the SOI (silicon-on-insulator) type, e.g., CMOS devices and bipolar transistors. Invented method avoids the use of difficult and complex epitaxial growth methods, uses commonly available semiconductor processing equipment and is compatible with normal Si IC processing.

Dwg.1/4

Title Terms: SILICON; POROUS; SILICON; PRODUCE; ANODISE; FOLLOW; ION; IMPLANT; PRODUCE; AMORPHOUS; STRUCTURE; SUIT; SOI; DEVICE
Index Terms/Additional Words: INSULATOR
Derwent Class: L03; U11; U13; U14
International Patent Class (Main): H01L-021/20; H01L-021/265; H01L-021/302; H01L-021/76
International Patent Class (Additional): C23C-014/48; H01L-021/321; H01L-021/336
File Segment: CPI; EPI
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Status: Signing Off...
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SILICON-ON-POROUS-SILICON; METHOD OF PRODUCTION AND MATERIAL

This invention relates to a method of producing silicon-on-porous-silicon material and to material and device production therefrom.

Porous silicon is a well known material (eg G Bomchil et al., Applied Surface Science 41/42 p604 1989). It can be obtained by anodic dissolution (anodizing) of silicon in hydrofluoric acid solutions. It is characterised by a network of fine pores, the number and size of which are determined by doping level of the silicon, dopant impurity type of the silicon and electrochemical parameters during anodizing. Subsequent oxidation of the porous silicon produces an insulating material.

Oxidized porous silicon provides one of the more promising materials for producing SOI (silicon-on-insulator) devices (eg N J Thomas et al., IEEE Device Letters 10(3) p129 1989; S S Tsao, IEEE Circuits and Devices Magazine p3 Nov.1987; K Imai and H Unno, IEEE Transactions on Electron Devices ED-31(3) p297 1984). There are two main methods of producing silicon-on-oxidised-porous-silicon. These are selective formation of porous silicon in order to isolate discrete silicon islands and direct epitaxial deposition on a porous silicon layer, each followed by oxidation of the porous silicon.

The latter of the two above methods has the practical disadvantage of requiring low temperature, minimum time, epitaxial growth conditions, in order to prevent restructuring the underlying porous silicon layer. This method is difficult to control when used for layers of thickness less than 0.25μm, and also expensive. For minimal, or zero, added defects the porous silicon must have a porosity of less than 50%. These porosity levels are difficult to achieve in any type of starting silicon material except in n^- n^+ and p^+. These types of starting material are not optimum for subsequent use in SOI device manufacture. Consequently, SOI material made by this technique uses non-optimum starting material and hence results in a higher than desirable defect density.

In general, the two most used techniques for the selective formation of porous silicon are the Full Isolation by Porous Silicon (FIPOS) p-n approach and the $n/n^+/n$ approach. FIPOS (K Imai, Solid State Electronics 24 p159 1981) uses implantation of protons to form temporary n-type silicon islands in p-type silicon wafers. Subsequently, the p-type silicon only is anodized such that porous silicon completely surrounds the temporary n-type silicon islands. Oxidation converts the temporary n-type silicon to p-type and the porous silicon to SiO_2. This technique suffers from a number of inherent disadvantages including those of wafer warpage due to lattice expansion occurring when the p-type porous silicon is oxidised, and also the presence of a thickness non-uniformity located at the centre of the islands. The non-uniformities inter alia induce dislocations within the islands and thus reduce electrical conformity of the n-type silicon.

The above problems were largely overcome by the use of the $n/n^+/n$ technique, where a thin epitaxial layer of n^- silicon is grown on either a n^+ doped epitaxial layer of silicon or onto a buried n^+ silicon diffusion layer. This method minimises wafer warpage, due to a creation of thinner porous silicon layers, increases the dimensions of silicon islands for which isolation is possible, due to confinement of the porous silicon transformation to lateral dimensions, and eliminates the non-uniformity. This method requires state-of-the-art epitaxial low pressure chemical vapour phase deposition (LPCPD) techniques. Where this technique is used to grow submicron n^- layers, it is particularly difficult to control. Also measurement of layer thicknesses thinner than approximately 0.5μm poses a problem as available techniques (eg SIMS, cross-sectional TEM and spreading resistance measurement) are destructive. Another disadvantage of this technique is that the extent of lateral anodisation is restricted to 50μm.

It is the aim of this invention to provide an alternative method of producing silicon-on-porous-silicon material.

According to this invention a method of producing silicon-on-porous-silicon material comprises the steps of

(i) manufacturing a porous silicon layer on a suitable silicon wafer, such that the silicon wafer has a porous silicon surface and a non-porous silicon surface,

(ii) applying an implanted ion dose to at least a portion of the porous silicon surface such that the dose is sufficient to cause amorphization of porous silicon.

The invention is advantageous in that it provides a method of producing silicon-on-porous-silicon material which avoids the use of epitaxial growth techniques, uses commonly available semiconductor processing equipment, and is compatiblae with normal silicon integrated circuit processing.

The porous silicon layer can be produced by standard anodization techniques, typically whereby suitable wafers of silicon are placed in an anodization cell made up of two half cells, each half cell containing a continuously agitated electrolyte, such as aqueous hydrofluoric acid (HF) or ethanoic-HF. The wafer is then anodized by passing a current from an anode, through one of the half cells by means of the electrolyte, through the wafer which normally forms a barrier between the two half cells, through the second half cell and out of the anodization cell via a cathode.

Typically, the silicon wafer is made porous through only part of its thickness. The porous material forms as a layer from the surface in contact with the first half cell electrolyte and into the thickness of the wafer. The layer's outermost surface, ie the surface in contact with the electrolyte of the first half cell is termed the porous silicon surface of the wafer, whilst the wafer surface in contact with the electrolyte within the second half cell is termed the non-porous silicon surface. The surface containing the porous silicon surface can be entirely converted to porous silicon, or alternatively only a portion of the surface may be converted to porous silicon.

The composition of the electrolyte used, currents applied, anodization time and resistivity of the starting silicon wafer determine the scale

of porosity and depth of the porous silicon layer produced. A typical electrolyte is 40% HF and ethanol of equal volumes at 5.5 mA/cm^2. Anodising for 6 minutes results in a porous density of 1.17 gm/cm^3 to a depth of 2.6μm in a 0.015 Ω-cm n type silicon wafer. Suitable silicon wafers are n^+, p^+ and p^-. P^- wafers are normally subjected to a pre-anodization p^+ implant on the non-porous silicon surface and annealed in order to enhance uniformity of current flow through the wafer during anodization.

Step (ii) of the method requires typical doses of greater than 1 x 10^{14} ions/cm^2 (at implant energies dependent upon the type of ion used), be applied to at least a portion of the porous silicon surface. The ion implantation may be carried out at room temperature or higher temperatures, such as 500°C. Typical suitable ions for single ion implantation are As^+, Ge^+, Si^+ and Sn^+, or for two successive ion implantations, F^+ followed by Ge^+, Si^+ or Sn^+ or vice versa. A preferred ion implantation programme is that of 1x10^{16} Ge^+/cm^2 at 80 keV followed by a 1x10^{16} F^+/cm^2 at 35 keV, both carried out at 500°C. Ion implantation with high enough doses induces amorphisation into the depth of the porous silicon layer. Thus amorphised silicon is produced from the porous silicon surface into the depth of the porous silicon layer such that the combined depth of the amorphised silicon and the reduced depth porous silicon is approximately equal to the porous silicon layer prior to amorphisation. Alternatively, the entire depth of the porous silicon layer can be amorphised, in which case the reduced depth porous silicon layer is not present.

Ion implantation is carried out preferably at incidence angles that minimise channelling of the ions down pores or major crystallographic axes. A typical standard industrially used angle of incidence is 7° (ie 7° away from normal incidence to the porous silicon surface). Other preferred angles of incidence are 83° and 15°. Other factors which influence the optimum angles of incidence include the degree of porosity and size of pores within the porous silicon layer. It is also common for some ion implantation wafer holders to impart up to about ±1° variation in implantation incidence angle from that normally stipulated.

Step (ii) can be carried out by applying an implanted ion dose to all or part of the porous silicon surface. Where the dose is applied to all the porous silicon surface, then the amorphised silicon forms as an amorphised silicon layer on a reduced depth porous silicon layer, unless the entire depth of the porous silicon is amorphised in which case the reduced depth porous silicon layer is not present. However, where the porous silicon surface is masked, eg with photoresist, such that only part of the porous silicon surface is exposed to the ion implanted dose, then amorphous silicon will be produced into the depth of the porous silicon layer from only those parts of the porous silicon surface which are unmasked. Use of masking in the manner described above results in amorphous silicon islands on the porous silicon surface, which have a depth into the porous silicon layer.

Material produced by the method of the invention is suitable for devices such as pyroelectric devices, where the porous silicon has a smaller thermal conductivity than bulk silicon.

A preferred method is that where steps (i) and (ii) are followed by step (iii), where step (iii) is that of recrystallizing the amorphous silicon. A preferred method of recrystallization is that of annealing. Typical annealing programmes include annealing temperatures of greater than 350°C for times dependent upon the annealing temperature, or annealing temperatures, used. Preferred annealing programmes include those of a 3 minute rapid thermal anneal at 950°C in argon and also 24 hours at 525°C in flowing nitrogen or argon.

Step (iii) can, where desired, be followed by other steps. In order to produce SOI material suitable for SOI device manufacture, these further steps include those of

(iv) patterning the recrystallized silicon, and

(v) oxidation of porous silicon to produce oxidised porous silicon.

Step (iv) is preferably carried out with knowledge of the type and dimensions of the SOI devices to be made subsequently from the SOI material.

Alternatively, step (v) can be carried out without recrystallization of the porous silicon. Such material would also be suitable for devices such as pyroelectric devices.

Step (iii) can also be preceded by a step where patterning of the amorphous silicon is carried out and include a step after step (iii) where the porous silicon is oxidised or partially oxidised. Patterning of the recrystallized silicon and of the amorphous silicon can be achieved by methods including those of standard lithographic masking and etching techniques. Patterning of the amorphous silicon or recrystallized silicon results in amorphous silicon or recrystallized silicon islands respectively.

Oxidation of the porous silicon is preferably carried out after a stabilizing oxidation. A stabilizing oxidation inhibits the restructuring of the porous silicon. A typical stabilizing oxidation is that of annealing the wafer at 300°C for 1 hour in flowing oxygen. This is thought to grow an oxide layer of about 1 monolayer thickness as a lining for the pores. Typically, a stabilizing oxidation would be carried out just prior to oxidation of the porous silicon. Alternatively, it can be carried out after patterning the amorphous silicon, prior to recrystallizing the amorphous silicon or after patterning the recrystallized silicon.

Where a stabilizing oxidation has been applied to the wafer, then a typical oxidation programme includes the steps of a 800°C wet oxidation for 2 hours, followed by 1090°C wet oxidation for 4 minutes and an optional final step of densification by annealing at a temperature of between about 1150°C and 1400°C for a time of between 24 hours and 1 hour respectively. A typical wet oxidation is a pyrogenic process in a wet ambient where H_2 and O_2 are burnt to give off excess O_2 in a steam vapour.

The 800°C wet oxidation produces a sufficient degree of oxidation, but gives a hydrated oxide. This hydrated oxide is termed "leaky" ie it is an oxide with higher conductivity than would be grown in similar conditions on bulk silicon. The 1090°C wet oxidation or annealing at temperatures of greater than 1000°C changes the "leaky" oxide to

oxidised porous silicon which behaves substantially like a thermally grown oxide. Preferably the oxidation is completed by densification, which is carried out in order to inhibit the dissolution of oxidised porous silicon which could otherwise occur during standard SOI device manufacture.

Steps (i) and (ii) can also be followed by metallization of the porous silicon. Thus, where the amorphous silicon forms a skin layer on the porous silicon layer the porous silicon is accessed by eg standard masking and etching techniques. Where the amorphous silicon is formed as islands on the surface of the porous silicon layer, then there is surface access to the porous silicon for metallization. Metallization is a known technique (eg S S Tsao et al., Applied Physics Letters 49(7) p403 1988; T Ito et al., Applied Surface Science 33/34 p1127 1988) and typically metals such as tungsten in a gaseous form are applied to the silicon-on-porous-silicon using LPCVD techniques at elevated temperatures. The porous silicon preferentially takes up the metal and is substantially completely converted to metal whilst the porous silicon is removed in vapour form. The resulting silicon-on-metal material may be used for devices where buried channels or buried contacts are required.

In order that the invention be more fully understood, it will now be described by example only and with reference to the accompanying figures, in which:

Figure 1 is a flow diagram including processing steps for carrying out the invention to produce silicon-on-porous-silicon material and SOI material.

Figure 2 is a schematic diagram of the changes made to a silicon wafer during the processing steps of Route B of Figure 1.

Figure 3 is a schematic diagram of the changes made to a silicon wafer during the processing steps of Route C of Figure 1.

Figure 4 is a schematic diagram of the changes made to a silicon wafer during the processing steps of Route A, where masking is employed to produce amorphous silicon islands.

As may be seen in Figure 1, Routes A and B describe the processing steps to be followed to produce silicon-on-porous-silicon. Route A results in silicon-on-porous-silicon in the form of amorphous silicon on porous silicon, whilst Route B results in silicon-on-porous-silicon in the form of recrystallized silicon on porous silicon. Figure 2 also outlines the processing steps of Route B of Figure 1 and Figure 4 describes the processing steps for Route A, where the amorphous silicon is produced as amorphous silicon islands.

As outlined in Figure 2 a three inch Czochralski-grown n^+ silicon wafer 1 (of dopant density 2.3×10^{16} cm^{-3} and resistivity of about 0.015Ω-cm) is placed in anodization equipment such as that described by patent application number GB 8923.709. The wafer is anodized at a current density of 5.5 mA/cm^2 in an electrolyte consisting of equal volumes of 40% HF and ethanol, resulting in anodized wafer 3 havibg porous silicon layer 2 and silicon substrate 4. After anodization for 6 minutes, the process produces a porous silicon layer 2.6 μm thick where the porous silicon layer has a porous density of 1.17 gm/cm^3 ie a porosity of 50%. Pores in such a porous silicon layer have sizes of about 4.24 nm, as measured by the BET technique, which is a gas adsorption/desorption technique. After anodization the anodised wafer 3 is removed from the anodization apparatus, rinsed with deionised water and spun dry. The wafer now has a porous silicon surface 5 and a non-porous silicon surface 6.

The anodized wafer 3 is then placed in a sample holder of an ion implanter, with the non-porous silicon surface 6 in contact with the sample holder. The anodised wafer and sample holder are then set up such that bombardment of the porous silicon surface 5 by ions is at an incidence of about 7° (with allowances for up to $\pm 1°$ variation due to induced wafer bending imparted by some sample holders). After evacuating the ion implanter and heating the sample holder to 500°C, the porous silicon surface 5 is bombarded by firstly Ge^+ with an energy of 80 keV to a dose level of 1×10^{16} cm^{-3} and secondly by F^+ ions at an

energy level of 35 keV to a dosage level of $1x10^{16}$ cm^{-3}. The ion implantation process as described above and with reference to Figure 2 provides an amorphous silicon skin layer 7 of 0.3 μm depth and a porous silicon layer 8, where the porous silicon layer 8 and the amorphous silicon layer 7 have a combined depth substantially equal to the depth of the porous silicon layer 2 . Where only a portion of the porous silicon surface 5 is accessible to the bombardment of implanted ions (due to eg previous masking), then amorphous silicon islands are formed in the porous silicon layer 2.

After ion implantation to form the amorphous silicon skin layer 7, the silicon-on-porous-silicon material produced by the Route described above can be further processed by carrying out step (iii), where step (iii) is recrystallization of the amorphous silicon. The addition of step (iii) to Route A is denoted as Route B on Figure 1.

Recrystallization of silicon skin layer 7 is achieved by annealing. Typical annealing programmes 3 minutes of rapid thermal annealing at 950°C in an argon environment, or a 24 hour anneal at 525°C in a nitrogen environment. The recrystallization produces a substantially single crystal recrystallized silicon layer 9 on the porous silicon layer 8.

The silicon-on-porous-silicon produced by Route B of Figures 1 and 2 can then be used for the manufacture of SOI material. SOI devices require a thin layer of silicon on an insulator. For fully depleted (ie the channel region of the device becomes majority carrier free) thin film CMOS devices the silicon layer needs to be less than 0.25 μm thick. Silicon-on-porous-silicon material produced by Route B above is particularly suited for SOI device manufacture as it is possible to use this method to produce a silicon layer thin enough for SOI device requirements. Alternatively the silicon-on-porous-material produced by the methods of Routes A and B can be used as base material for further epitaxial growth and also as material suitable for metallisation by eg Tungsten.

Figure 3 is a schematic diagram showing additional method steps that can be carried out on the silicon-on-porous-silicon material produced by Route B in order to produce SOI material. The processing steps shown in Figure 3 are denoted as Route C in Figure 1.

As outlined in Figure 3, silicon island definition follows the manufacture of silicon-on-porous-silicon by Route B. Such definition may be carried out to provide standard island morphologies, or preferably to provide morphologies specifically required for particular device manufacture.

Silicon island definition is commonly carried out by photolithography and dry etching, in order to selectively etch away unwanted silicon material. Typically such a process would involve covering the recrystallized silicon surface 10 with photoresist, selectively exposing the photoresist which covers areas of unwanted recrystallized silicon to U-V radiation by means off masking off required areas of recrystallized silicon, and selectively dry etching away the unwanted recrystallized silicon whilst photoresist protects the required areas of recrystallized silicon. The required areas of recrystallized silicon are device islands 20.

After device island patterning, the porous silicon layer 8 undergoes a stabilizing oxidation. Such an oxidation is often used to protect porous silicon from being restructured during subsequent processing steps requiring elevated temperatures. A typical stabilizing oxidation programme anneals the anodized wafer 3 at 300°C for 1 hour in an oxygen ambient. Such a programme is thought to grow an oxide layer of about one monolayer thickness as a lining of the pores within the porous silicon layer to produce a stabilized, partially oxidised, porous silicon layer 21.

After a stabilizing oxidation an oxidation programme can be carried out. A typical oxidation programme includes the steps of a 800°C wet oxidation for 2 hours, followed by a 1090°C wet oxidation for 6 minutes and an optional final step of densification by typically annealing at a temperature of between 1150°C and 1400° for a time of between 24 hours and 1 hour respectively. A typical wet oxidation is a pyrogenic process

in a wet ambient where H_2 and O_2 are burnt to give off excess O_2 in a steam vapour.

The 800°C oxidation produces a sufficient degree of oxidation, but is hydrated. This gives a "leaky" oxide. The 1090°C wet oxidation changes the "leaky" oxide to give oxidised porous silicon layer 22, which behaves substantially like a thermally grown oxide. Densification is carried out in order to inhibit the dissolution of the oxidised porous silicon layer 22, which could otherwise occur during SOI device standard manufacture.

Following oxidation, removal of excess oxide 23 formed during oxidation leads to silicon (in the form of device islands 20) on insulator (in the form of oxidised porous silicon layer 22) material.

As can be seen from Figure 1, Route C is not the only manufacturing method by which SOI material can be obtained. Other typical Routes include those shown as Routes D and E on Figure 1. SOI device manufacture can be carried out on the SOI material obtained by the production methods as described by Figure 1 by such well known production technologies as eg ion implantation etc. Typical SOI devices for which such SOI material may be used include C-MOS and bipolar devices.

Material produced by Route A can alternatively be produced where only a portion of the porous silicon surface is bombarded with an implanted ion dose which is sufficient to amorphise porous silicon. A schematic representation of the above production method may be seen in Figure 4. Wafer 1 is anodized in the manner described above, such that the anodized wafer 3 has a porous silicon layer 2 on a substrate 4, with porous silicon surface 5 and non-porous silicon surface 6. A layer of photoresist 30 is then spun on the porous silicon surface. Photoresist covering selected areas of the porous silicon surface is then exposed to U-V radiation. Subsequent etching of the photoresist with a suitable etchant results in the selected areas of the porous silicon surface being revealed, whilst non-selected areas of the porous silicon surface remain masked by the remaining photoresist. The anodized wafer is then ion implanted as described above with reference to Figure 2, resulting

in amorphous silicon islands 31 extending into the depth of the porous silicon layer from the portion of the porous silicon surface not masked by the photoresist. Stripping away of the resist covering the non-selected areas of the porous silicon surface gives amorphous-silicon-on-porous-silicon material.

The material produced by the method described by Route A and Figure 4 can be used for inter alia the manufacture of metallized material by eg Tungsten, recrystallized-silicon-on-porous-silicon material, SOI material obtained by eg the methods described above with reference to Figures 2 and 3 and also devices such as pyroelectric, SOI C-MOS and SOI bipolar devices.

CLAIMS.

1. A method of producing silicon-on-porous-silicon comprising the steps of

(i) manufacturing a porous silicon layer on a suitable silicon wafer, such that the silicon wafer has a porous silicon surface and a non-porous silicon surface.

(ii) applying an implanted ion dose to at least a portion of the porous silicon surface such that the dose is sufficient to cause amorphisation of porous silicon.

2. A method according to claim 1 where the implanted ion dose is greater than $1x10^{14}$ ions/cm^2.

3. A method according to either of the preceding claims where the ion implantation is carried out at room temperature.

4. A method according to any of the preceding claims where the ion implantation is carried out with a single species of ion.

5. A method according to claim 4 where the single species of ion is taken from the list of As^+, Ge^+, Si^+ and Sn^+.

6. A method according to any of claims 1 to 3 where the ion implantation is carried out with two successive ion implantations.

7. A method according to claim 6 where the successive ion implantations are carried out with F^+ followed by an ion taken from the list of Ge^+, Si^+ and Sn^+.

8. A method according to claim 6 where the successive ion implantations are carried out with one ion taken from the list of Ge^+, Si^+ and Sn^+ followed by F^+.

9. A method according to any of the preceding claims where the ion dose is implanted at an angle of incidence 7°±.

10. A method according to any of the preceding claims where the ion implantation dose is applied to at least a portion of the porous silicon surface.

11. A method according to any of the preceding claims where the amorphous silicon is recrystallized.

12. A method according to claim 11 where the recrystallization is achieved by annealing.

13. A method according to claim 12 where the annealing temperature is greater than 350°C.

14. A method according to any of the preceding claims where the porous silicon is metallised.

15. A method of any of the preceding claims where the silicon of the silicon-on-porous-silicon is patterned.

16. A method according to any of the preceding claims and further comprising a step of carrying out a stabilizing oxidation of the porous silicon.

17. A method according to claim 16 where the stabilizing oxidation is carried out prior to patterning of the silicon.

18. A method according to any of the preceding claims and further comprising a step where the porous silicon is at least partially oxidised.

19. A method according to claim 18 where the oxidation is carried out after a method according to any of claims 16 and 17.

20. A method according to any of claims 18 and 19 and further comprising a densification step.

21. A semiconductor device manufactured from material as claimed in any of the preceding claims.

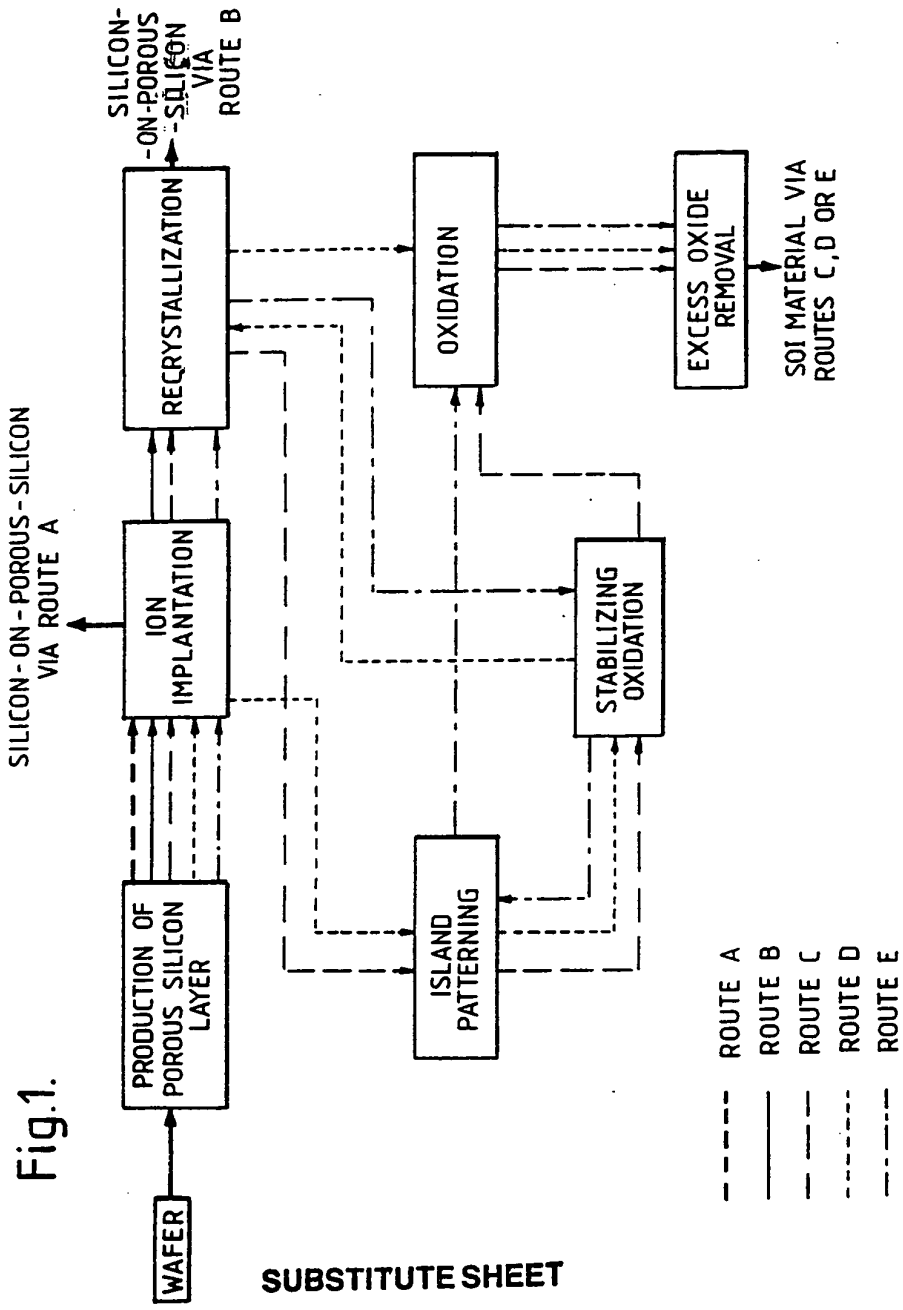
WAFER
PRODUCTION OF POROUS SILICON LAYER
ION IMPLANTATION
RECRYSTALLIZATION
SILICON-ON-POROUS-SILICON VIA ROUTE A
SILICON-ON-POROUS-SILICON VIA ROUTE B
ISLAND PATTERNING
STABILIZING OXIDATION
OXIDATION
EXCESS OXIDE REMOVAL
SOI MATERIAL VIA ROUTES C,D OR E
ROUTE A
ROUTE B
ROUTE C
ROUTE D
ROUTE E

Fig.1.

Fig.2.

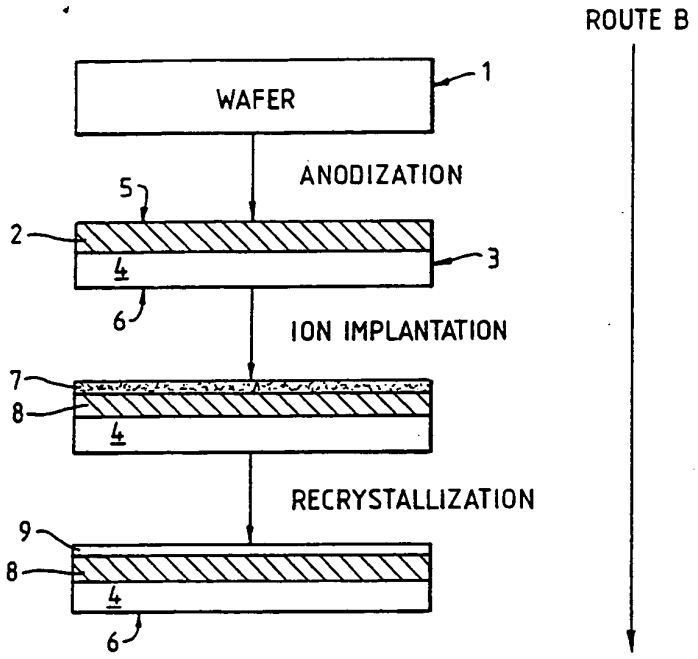
ROUTE B
WAFER
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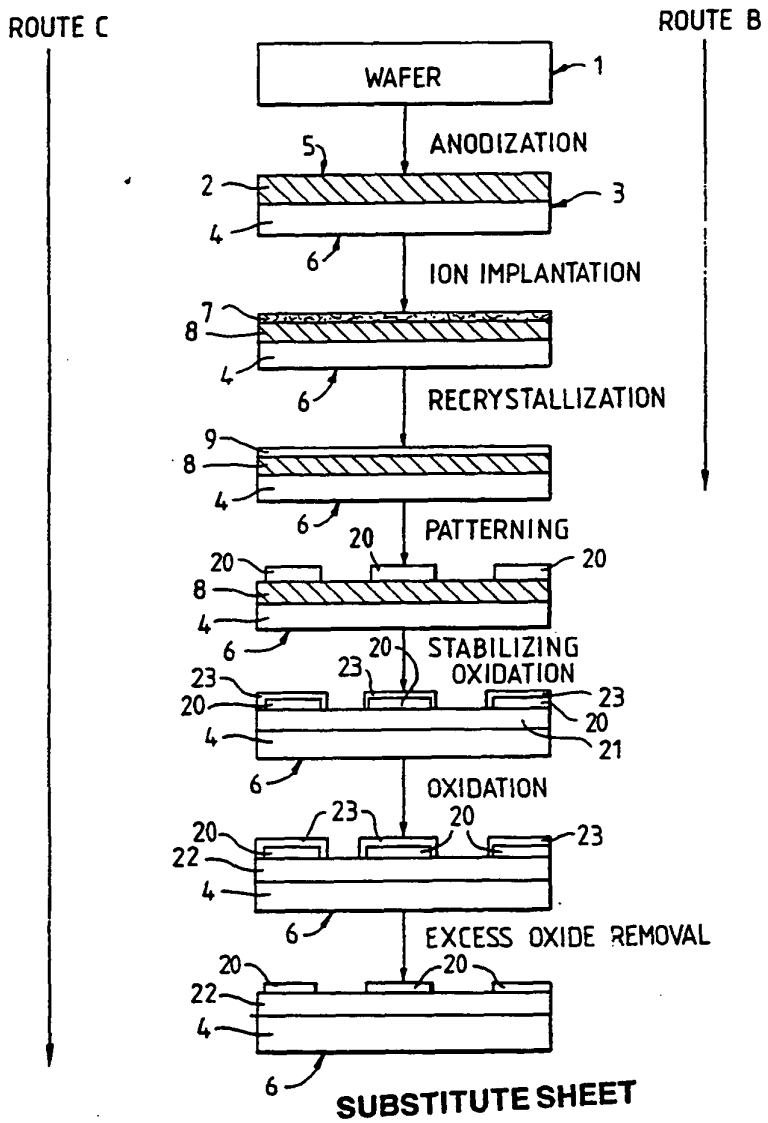
Fig.3.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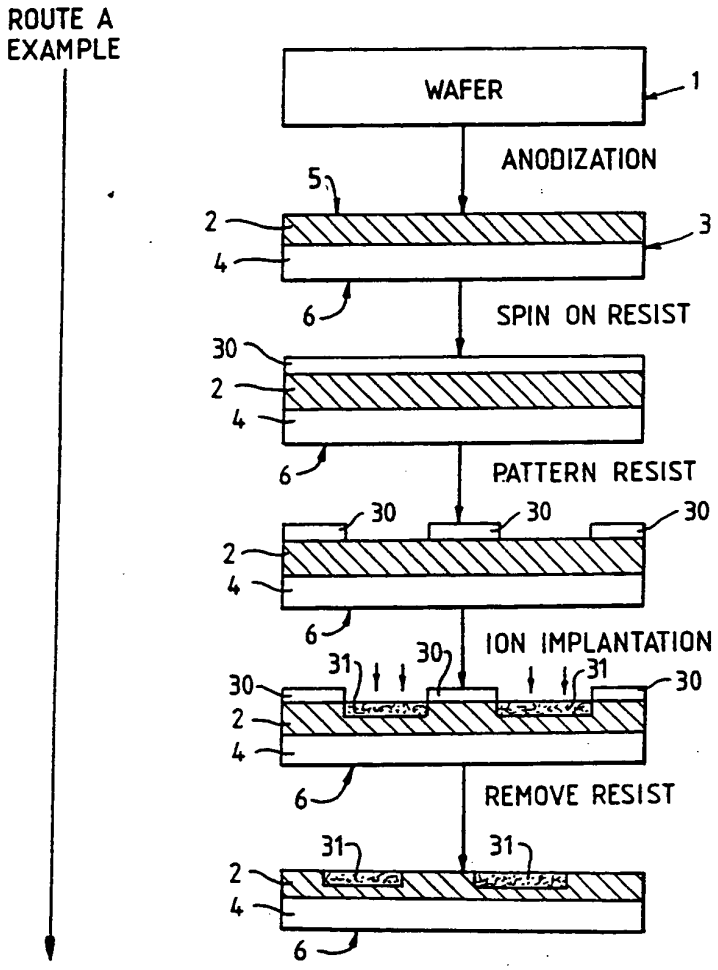
PATTERNING
20
STABILIZING OXIDATION
23
21
OXIDATION
22
EXCESS OXIDE REMOVAL

Fig.4.


ROUTE A
EXAMPLE
WAFER
1
ANODIZATION
5
2
3
4
6
SPIN ON RESIST
30
PATTERN RESIST
ION IMPLANTATION
31
REMOVE RESIST

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 H01L21/76; H01L21/265; H01L21/20; H01L21/321

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	H01L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No.[13]
X	EP,A,0 312 466 (ETAT FRANCAIS (CNET)) 19 April 1989 see column 3, line 29 - column 3, line 65; claims 1,2; figure 4	1,10-13, 16,1820, 21
A	NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH, SECTION -B vol. 19/20, no. 1, February 1987, AMSTERDAM pages 307 - 311; J. THORTON ET AL.: 'AMORPHISATION OF SILICON BY BOMBARDMENT WITH GROUP IV IONS.' see the whole document	1-6, 11-13

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* Special categories of cited documents :[10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
31 JANUARY 1992	17.02.92
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	VANCRAEYNEST F.

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
A	JOURNAL OF APPLIED PHYSICS. vol. 58, no. 2, July 1985, NEW YORK US pages 683 - 687; T.E. SEIDEL ET AL.: 'RAPID THERMAL ANNEALING OF DOPANTS IMPLANTED INTO PREAMORPHIZED SILICON' see the whole document	1-8, 11-13
A	PATENT ABSTRACTS OF JAPAN vol. 8, no. 272 (E-284)(1709) 13 December 1984 & JP,A,59 144 149 (TOUKOU ET AL.) 18 August 1984 see abstract	1,11-15, 21

ANNEX TO THE INTERNATIONAL SEARCH REPORT
ON INTERNATIONAL PATENT APPLICATION NO. GB 9102029
SA 53314

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
The members are as contained in the European Patent Office EDP file on
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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A-0312466	19-04-89	FR-A- 2620571	17-03-89

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82